## IN THE CLAIMS

Please cancel claims 1-8, 11, 20-29, and 31.

Please amend claims 9, 12, and 13 as follows:

1-8. (Cancelled)

9. (Currently Amended) A memory comprising:

a clock stop detector for detecting a clock signal being not active for a predetermined period of time, the clock stop detector configured to receive the clock signal and output a control signal in response to the clock signal; ~~and~~

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal~~,~~; and

an address receiver configured to receive the control signal and activate and deactivate in response to the control signal,

wherein the clock stop detector comprises:

a first switch that closes in response to a first logic level of an inverted clock signal to charge a capacitor;

a second switch that closes in response to a second logic level of the inverted clock signal to discharge the capacitor; and

a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time,

wherein the capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and

wherein the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding the predetermined period of time.

10. (Original) The memory of claim 9, further comprising:

a clock receiver configured to receive an external clock signal and pass the clock signal to the clock stop detector.

11. (Cancelled)

12. (Currently Amended) ~~The~~ A memory ~~of claim 9, further~~ comprising:

a clock stop detector for detecting a clock signal being not active for a predetermined period of time, the clock stop detector configured to receive the clock signal and output a control signal in response to the clock signal;

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal; and

a command receiver configured to receive the control signal and activate and deactivate in response to the control signal,

wherein the clock stop detector comprises:

a first switch that closes in response to a first logic level of an inverted clock signal to charge a capacitor;

a second switch that closes in response to a second logic level of the inverted clock signal to discharge the capacitor; and

a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time,

wherein the capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and

wherein the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding the predetermined period of time.

13. (Currently Amended) ~~The~~ A memory ~~of claim 9~~comprising:~~,~~

a clock stop detector for detecting a clock signal being not active for a predetermined period of time, the clock stop detector configured to receive the clock signal and output a control signal in response to the clock signal;

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal; and

a data receiver and driver configured to receive the control signal and activate and deactivate in response to the control signal,

wherein the clock stop detector comprises:

a first switch that closes in response to a first logic level of an inverted clock signal to charge a capacitor;

a second switch that closes in response to a second logic level of the inverted clock signal to discharge the capacitor; and

a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time,

wherein the capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and

wherein the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding the predetermined period of time.

14. (Cancelled)

15. (Previously Presented) The memory of claim 9, wherein the first switch comprises a first transistor and the second switch comprises a second transistor.

16. (Original) The memory of claim 9, wherein the memory comprises a random access memory.

17. (Original) The memory of claim 9, wherein the memory comprises a dynamic random access memory.

18. (Original) The memory of claim 9, wherein the memory comprises a double data rate synchronous dynamic random access memory.

19. (Original) The memory of claim 9, wherein the memory comprises a mobile random access memory.

20-31. (Cancelled)

32. (Previously Presented) A memory comprising:

a clock stop detector configured to receive a clock signal and output a control signal in response to the clock signal;

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal; and

a data receiver and driver configured to receive the control signal and activate and deactivate in response to the control signal.

33-37. (Cancelled)

38. (Previously Presented) A memory comprising:

a clock stop detector configured to receive a clock signal and output a control signal in response to the clock signal;

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal; and

an address receiver configured to receive the control signal and activate and deactivate in response to the control signal.

39. (Previously Presented) A memory comprising:

a clock stop detector configured to receive a clock signal and output a control signal in response to the clock signal;

a peripheral circuit for reading and writing data to a memory bank, wherein the peripheral circuit is configured to receive the control signal and activate and deactivate in response to the control signal; and

a command receiver configured to receive the control signal and activate and deactivate in response to the control signal.